REMARKS

I. Introduction

In response to the pending Office Action, Applicants have cancelled claim 7, without prejudice, and amended claims 6, 8, 9 and 11 so as to more specifically define the intended subject matter of the present invention. Support for the amendments to claim 6 can be found, for example, in Figs. 4-6 and embodiments 3 and 4 as described in the specification. Support for new claim 23 can be found, for example, on page 18, line 27 – page 19, line 1, and support for new claim 24 can be found, for example, in Fig. 7 and the description of embodiment 5. No new matter has been added.

It is noted that two articles cited in an Information Disclosure Statement filed concurrently with the filing of the application, where not initialed in the PTO-1449 form returned with the instant Office Action. These references were cited in the parent application (USP Application Ser. No. 09/102,166). It is presumed that the failure to initial these references was an inadvertent omission. If for any reason the Examiner needs additional copies of these articles, it is respectfully requested that the Examiner contact the undersigned attorney.

For the reasons set forth below, it is respectfully submitted that all pending claims are patentable over the cited prior art.

II. The Rejection Of Claim 6 Under 35 U.S.C. § 112, S cond Paragraph

Claim 6 was rejected under 35 U.S.C. § 112, second paragraph, for failing to provide antecedent basis for all claim elements. Applicants have amended claim 6 so as to correct the lack of antecedent basis noted by the Examiner. It is respectfully submitted that the foregoing rejection overcomes the pending rejection.

III. The Rejection Of Claim 6 Under 35 U.S.C. § 102

Claim 6 was rejected under 35 U.S.C. § 102(e) as being anticipated by USP No. 6,292,202 to Nishio. For the reasons set forth below, it is respectfully submitted that amended claim 6 is not anticipated by Nishio.

As recited by amended claim 6, the present invention relates to a method of processing data in a semiconductor device comprising at least one memory array, a data processor and an internal data bus, which couples the memory array to the data processor. More specifically, in accordance with the method recited by claim 6, processing specification information and the data to be processed are written in a first area corresponding to a first word line and a second area corresponding to a second word line, respectively, where the first and second word lines are within the same semiconductor device coupled to the data processor via the internal bus. Then, the processing specification information and the data are transferred to the data processor via the internal bus. Next, the results obtained by the data processor are written into a

third area corresponding to a third word line within the semiconductor device via the internal bus.

As a result of the method of the present invention, it is possible to transfer information in parallel between a significant number of memory cells connected to the word lines and the data processor via the internal bus, which has a substantially wide bit width, thereby resulting in a significant decrease in the processing time.

Turning to the cited prior art, Nishio discloses a data processing method in which data to be processed, which is input from an external device, is written in a band memory B. The control unit subjects the data in band memory B to imaging processing based on received control information, and then stores the processed results in memory A. (*See*, Nishio, Abstract). However, Nishio appears to fail to disclose where the received control information, such as the band information or the attribute information table illustrated in Fig. 8, is written. Thus, at a minimum, Nishio fails to disclose that the processing specification information is written in a first area corresponding to a first word line within a semiconductor device comprising at least one memory array and a data processor coupled via an internal bus, as recited by claim 6.

Further, Nishio merely discloses that the data to be processed is written in the band memory B. There is no relationship between the band memory B and the destination where the processing specification information is written. Thus, Nishio also fails to disclose or suggest that the data to be processed is written in the second area

corresponding to a second word line, which is different from the first word line, within the semiconductor device, as recited by claim 6.

In addition, Nishio also fails to disclose or suggest any step corresponding to the step of "transferring the processing specification information through at least one internal data bus to the data processor" or the step of "transferring the data through at least one internal bus to the data processor", as recited by claim 6.

Finally, Nishio also appears to fail to disclose any step corresponding to the step of "writing resultant processed data through at least one internal data bus in a third area corresponding to a third word line within the semiconductor device", as recited by claim 6.

Thus, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for at least the foregoing reasons, it is clear that Nishio does not anticipate amended claim 6, or any claim dependent thereon.

IV. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc.***

Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0417. A duplicate copy of this Response is enclosed for accounting purposes.

Respectfully submitted,

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v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 6 is patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

V. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time. The